



# H61H2-M12

Rev : 1.0

ECS CONFIDENTIAL

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### NOTE:

Design by 428971\_428971\_Sugar\_Bay\_and\_BromolowWS\_PDG\_Rev\_0\_8.pdf,  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Rev1p0.zip

## REVISION HISTORY:

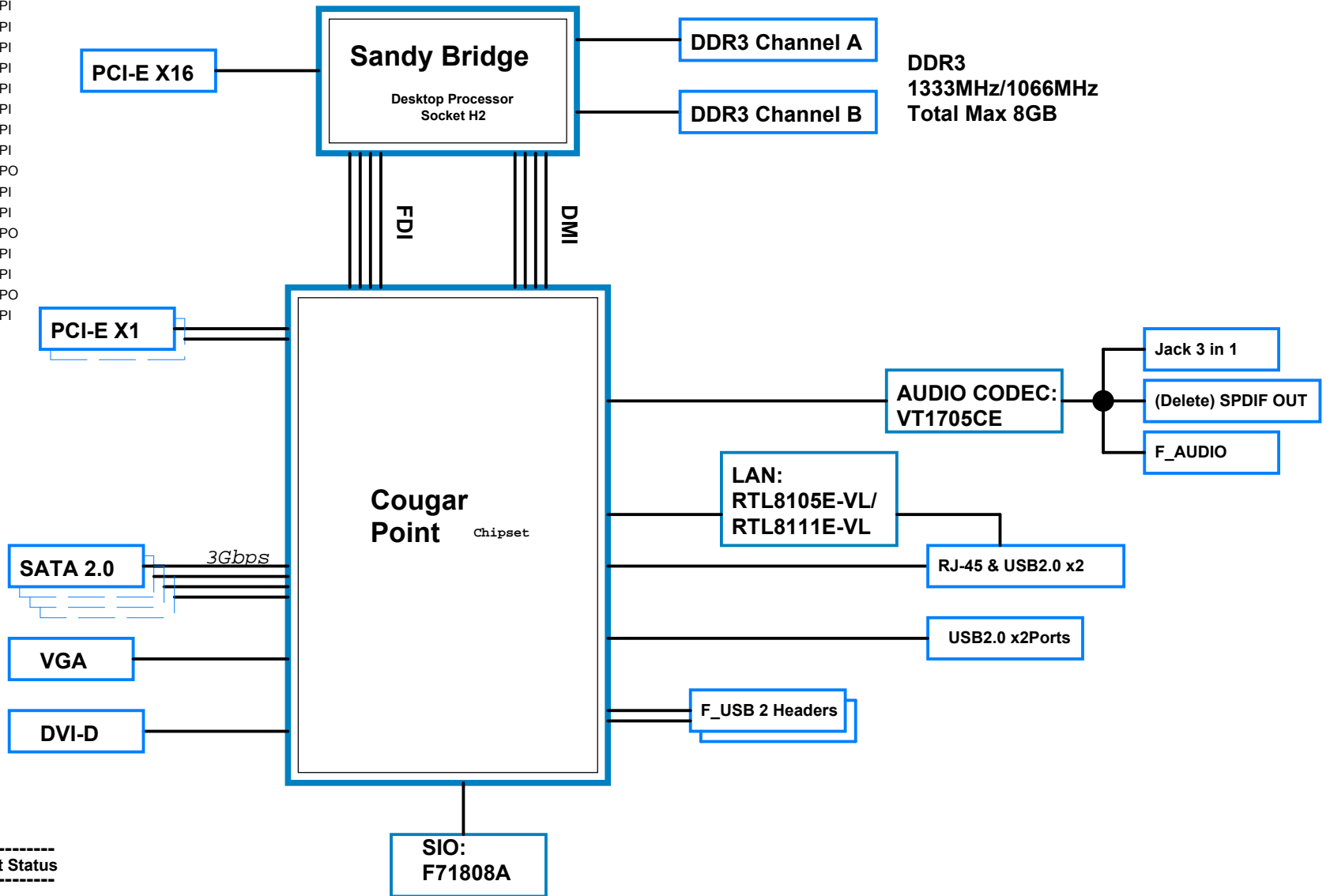
Rev	Date	Notes
P61G V1.0	2011/04/07	RED_PCB P/N : 15-Y97-011001 (GE1) / 15-Y97-011000 (CHUANYI) BOM P/N : 81-605-Y97100  EC35 change to EC-cap 1000U-6.3DL  EC1, EC4 from 100uF change to 220uF  Del RT1, RT3, R137, R180 ( Not need compensation of temperature ).  For 5VSB Inrush Current : R102 from 100k change to 33k.  Select TACH0_GPIO17 to decide COM .
H61H2-M12 VA	2011/05/04	Black_PCB P/N : 15-EC7-010010 BOM P/N : 81-605-EC7000/81-605-EC7001(10/100 ; GiGA)  PCB Size change to 225*170 mm  Del DVI  Vcore 減少一相  VIN 電容減少一顆  LAN change to Atheros 8152/8151/8161  Codec change to VT1705CE.  USB Power use fuse & Jumper.
H61H2-M12 V1.0	2011/07/12	Black_PCB P/N : 15-EC7-011000/15-EC7-011001 BOM P/N :  PCB Size change to 225*170 mm

RD : Jayson  
LAYOUT :  
EMI :

 Elitegroup Computer Systems			
Title			
Cover Page			
Size	Document Number	Rev	
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## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI
GPIO15	3VSB	Down Voltage for DIMM	GPO
GPIO48	VCC3	Down Voltage for DIMM	GPI



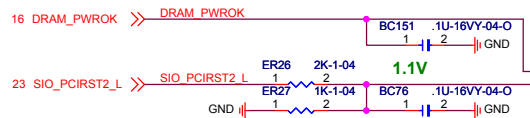
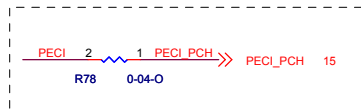
**DDR3**  
1333MHz/1066MHz  
Total Max 8GB

## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
PIN23	5VSB	Power LED	GPIO25/LEDVCC/WDTRST#
PIN22	5VSB	Power LED	GPIO24/LEDVSB
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)





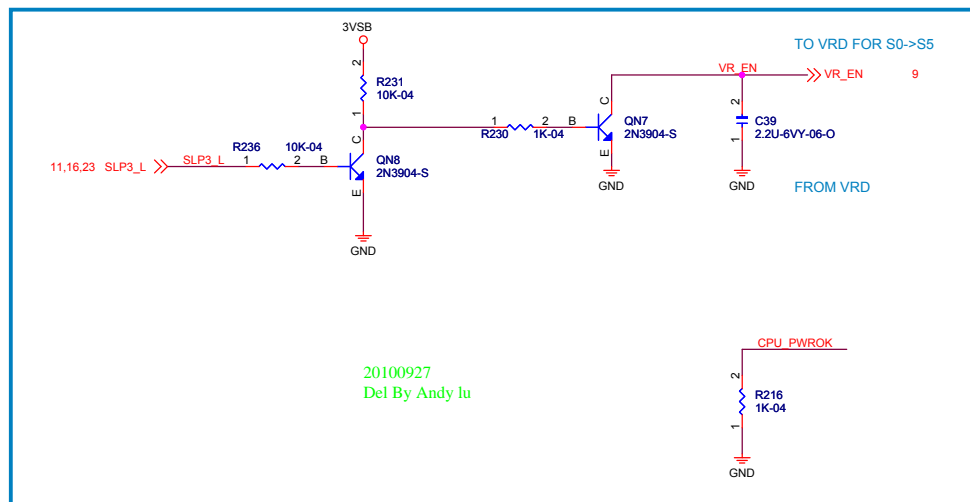
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

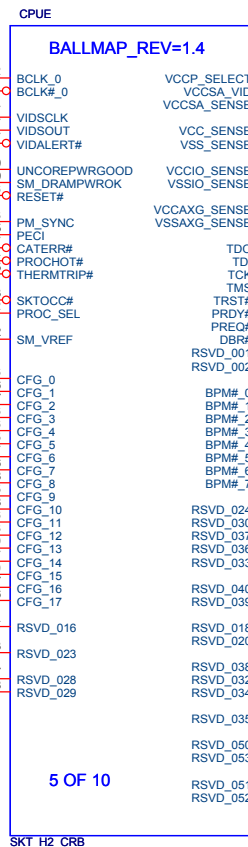
CFG[5:6]:  
 01=DEFAULT X16,  
 01=2X8,  
 10=RESERVED,  
 00=X8,X4,X2

## Power Down Sequencing Circuit

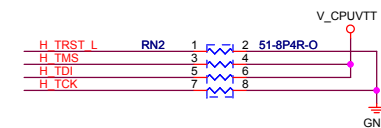


20100927  
 Del By Andy lu

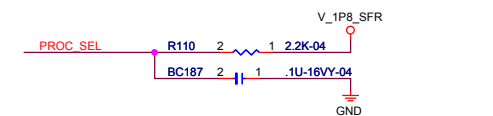
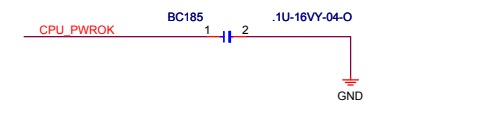
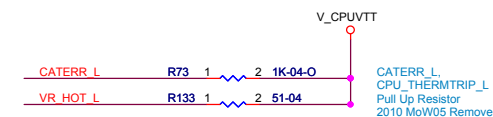
change test point for internal PU Jack05/25



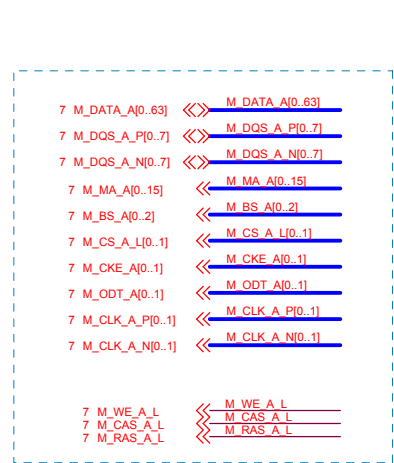
1130-10  
 pull high By Jayson Del,  
 Pull high on Hage11



EDS P68/132 has internal PU Jack05/25

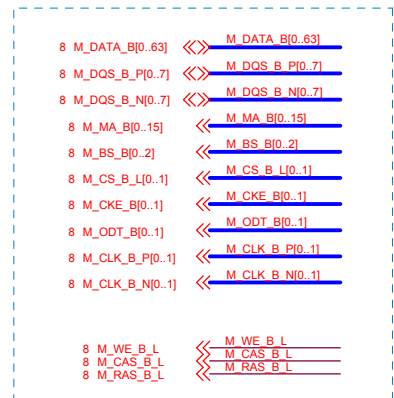


DMI/FDI termination voltage:  
 DC coupled: TX/RX to VCC ISF sampled high  
 DC coupled: TX/RX to VSS IF sampled low  
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

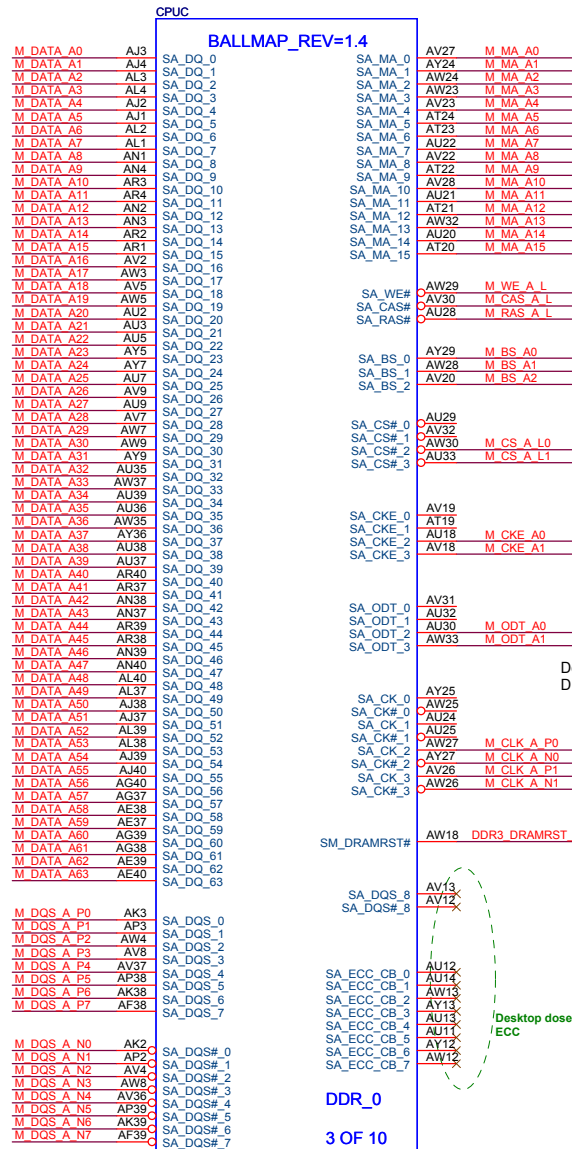


DDR3 CH.A

7,8 DDR3\_DRAMRST\_L << DDR3\_DRAMRST\_L



DDR3 CH.B



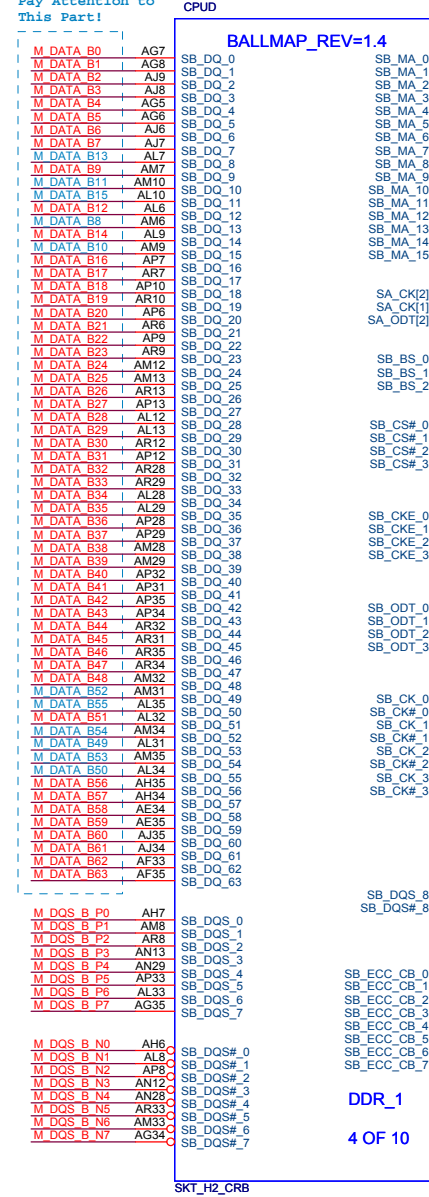
DDR\_0

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SKT\_H2\_CRB

DDR3 CH.A

Pay Attention to This Part!



DDR\_1

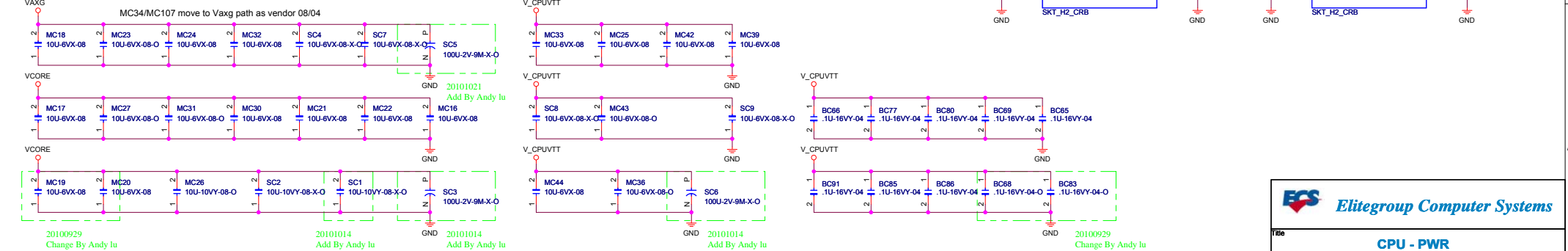
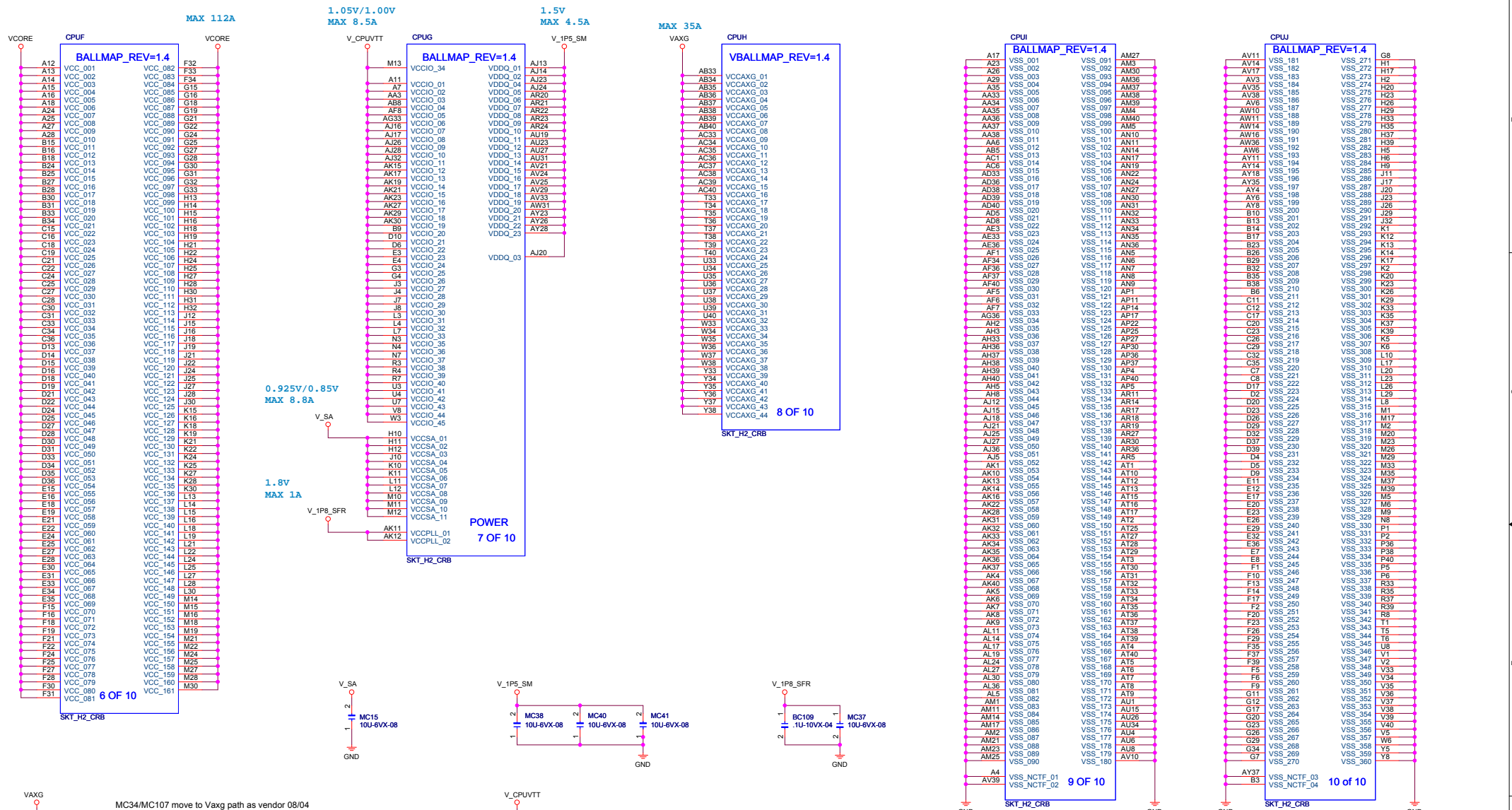
4 OF 10

SKT\_H2\_CRB

DDR3 CH.B



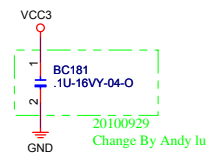
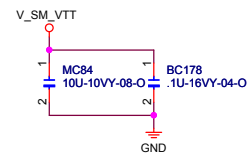
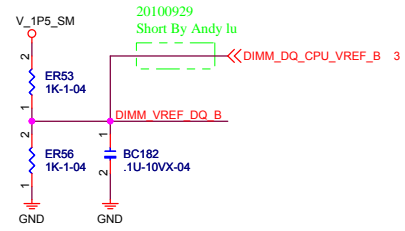
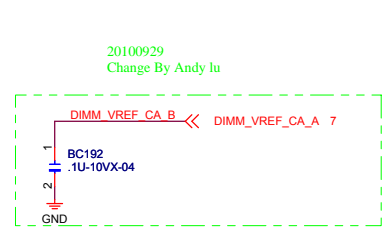
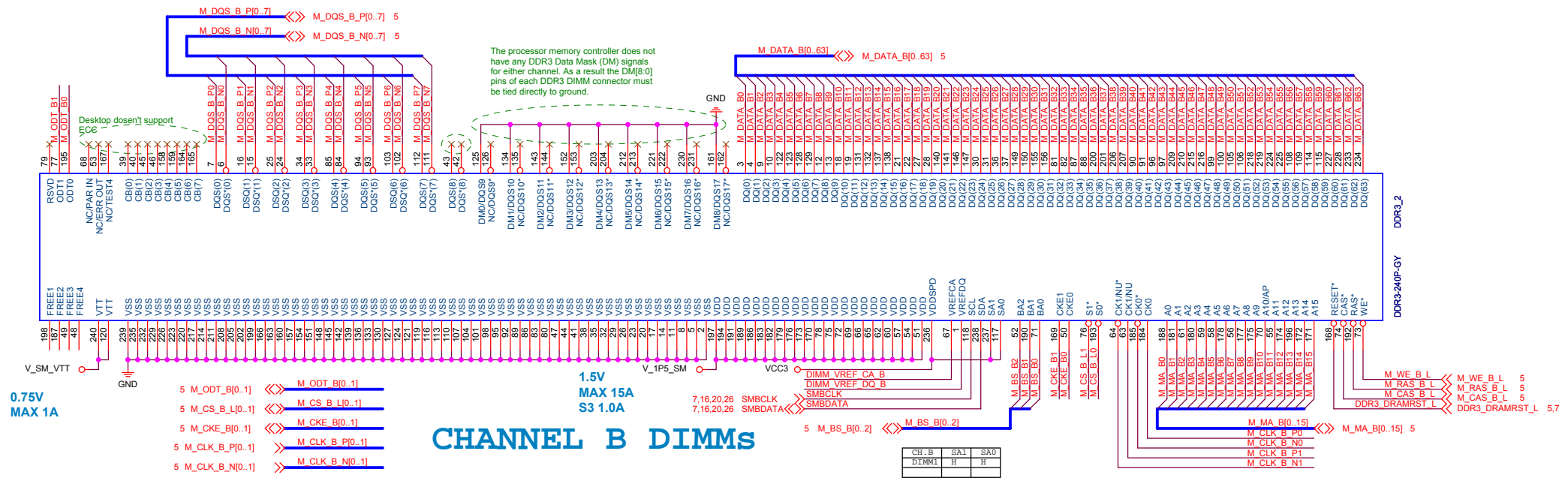
Elitegroup Computer Systems







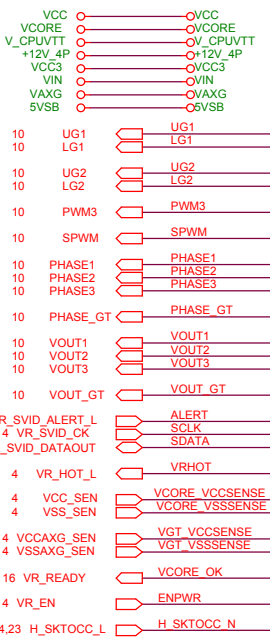
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



Del DIMM3 for always populate DIMM4 first Jack 05/13



## External Connection



Css connect from DAC to FBRTN for SS and Dynamic VID.  
 $T_{ss} = T_{dynamic} = V_{DAC} * C_{ss} / I_{ss}$ ,  $V_{boot} = 0$   
 $T_{ss} = (V_{DAC} - V_{boot}) * C_{ss} / I_{ss}$ ,  $V_{boot} \neq 0$   
 $I_{ss} = 200\mu A$ , if SETVID = Fast (01H)  
 $I_{ss} = 50\mu A$ , if SETVID = Slow (02H)

Load Line =  $DCR * R_{DRP} / (n * R_{csn})$   
 $R_{DRP}$   
 $V_{EAP} = V_{DAC} - I_{sum} * D_{DRP}$   
 $V_{DAC} = SetVID + Offset$

$V_{IMON} = I_{sum} * R_{IMON}$   
 $I_{sum} = I_o * DCR / (n * R_{csn})$   
 OCP set  
 Phase Frequency:  
 $f_{sw} = 300 * (27k / RT) * 0.83$   
 $RT = 25k \rightarrow f_{sw} = 300k Hz$

1202'10 Jayson :  
Vendor 先預留不上.

1230'10 for uP1625P


RT Close to L7

0105'11:  
Del R170 due to P23  
has pulled up.  
20100929  
Change By Andy lu

uT501

VBOOT :  
 VCC -> VCORE / VAXG boot 1.1V  
 GND -> VCORE / VAXG boot 0V

POR condition :  $VCC5 > 4.3V$  AND  $VCC12 > 9.5V$  AND  $ENPWR > 0.65V$   
 OCP condition :  $V_{IMON} > 1.3 * V_{IMAX}$  for total current  
 $I_{CSNx} > 100\mu A$  for channel current  
 OVP condition :  $V_{FB} - V_{EAP} > 150mV$   
 UVP condition :  $V_{FB} < 200mV$


**Elitegroup Computer Systems**

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Size	Document Number	H61H2-M12	
Customer			Rev 1.0
Date:	Wednesday, July 13, 2011	Sheet	9 of 29

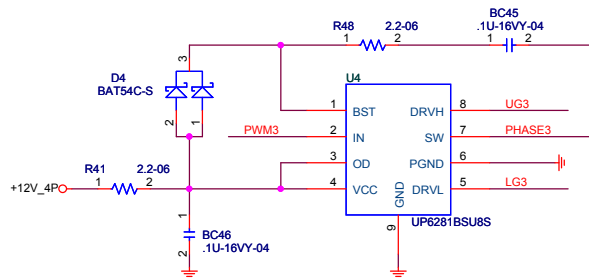
## External Connection

VCC  
VCORE  
VAXG  
+12V\_4P  
VCC3  
VIN

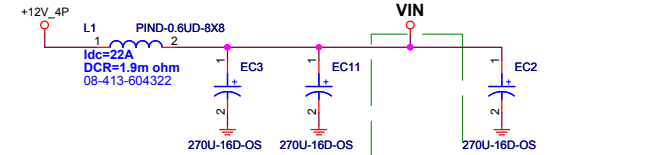
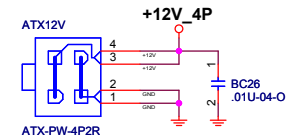
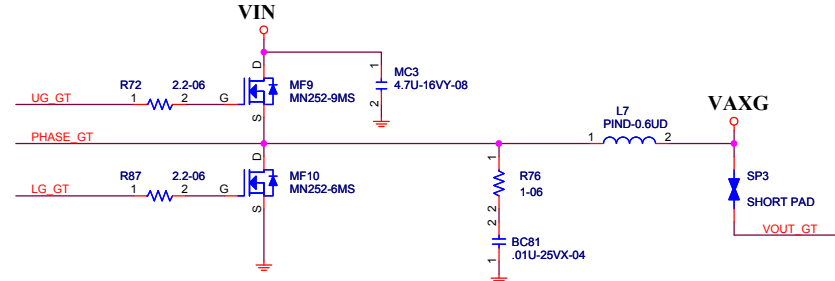
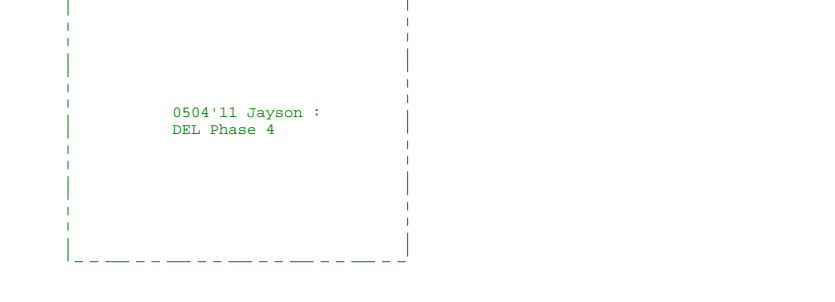
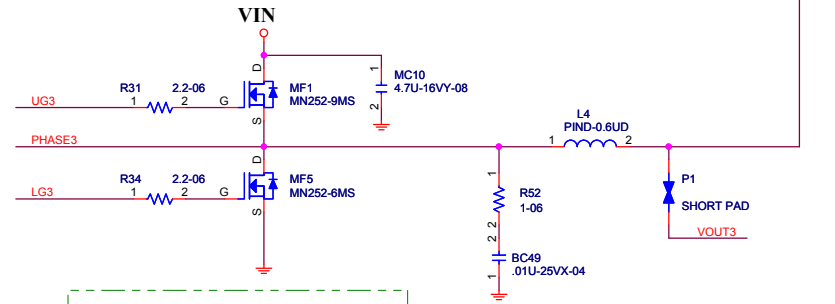
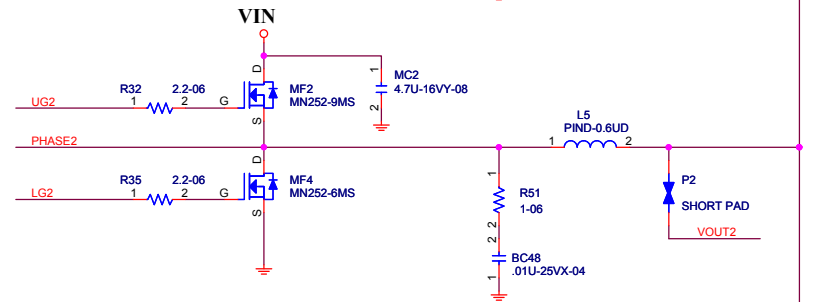
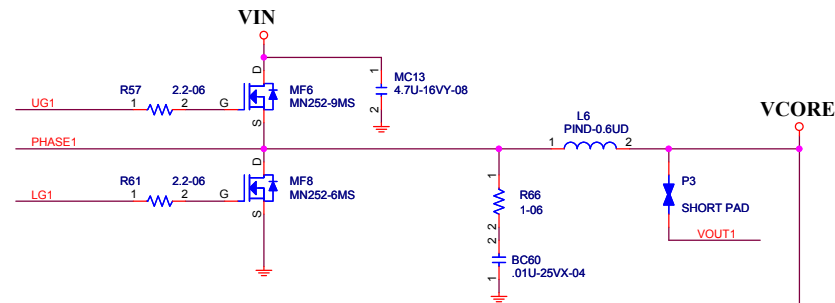
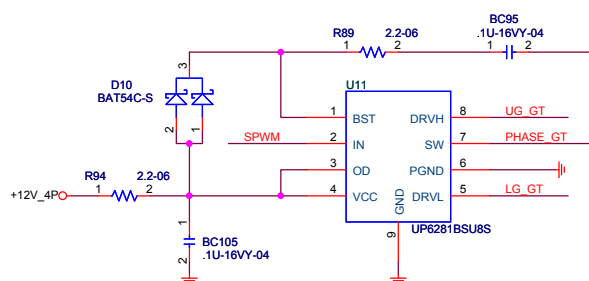
9 UG1  
9 LG1  
9 UG2  
9 LG2  
9 PWM3  
9 SPWM

9 PHASE1  
9 PHASE2  
9 PHASE3  
9 PHASE\_GT

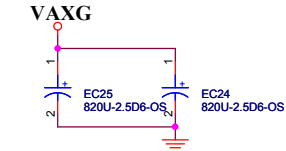
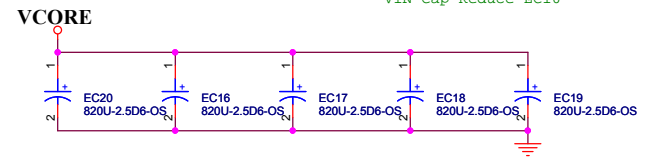
9 VOUT1  
9 VOUT2  
9 VOUT3  
9 VOUT\_GT



0504'11 Jayson :  
DEL Driver



0504'11 Jayson :  
VIN Cap Reduce EC10



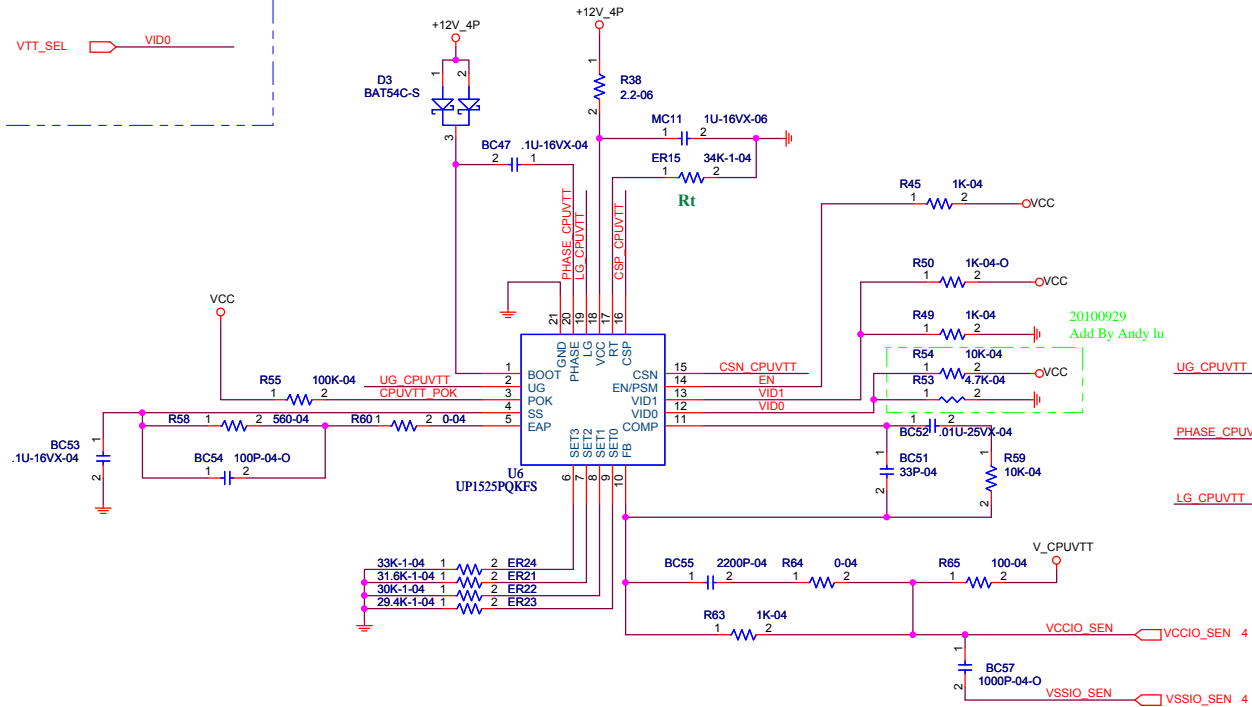
Elitegroup Computer Systems

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Size	Document Number	H61H2-M12	
Custom		Rev	1.0
Date:	Wednesday, July 13, 2011	Sheet	10 of 29

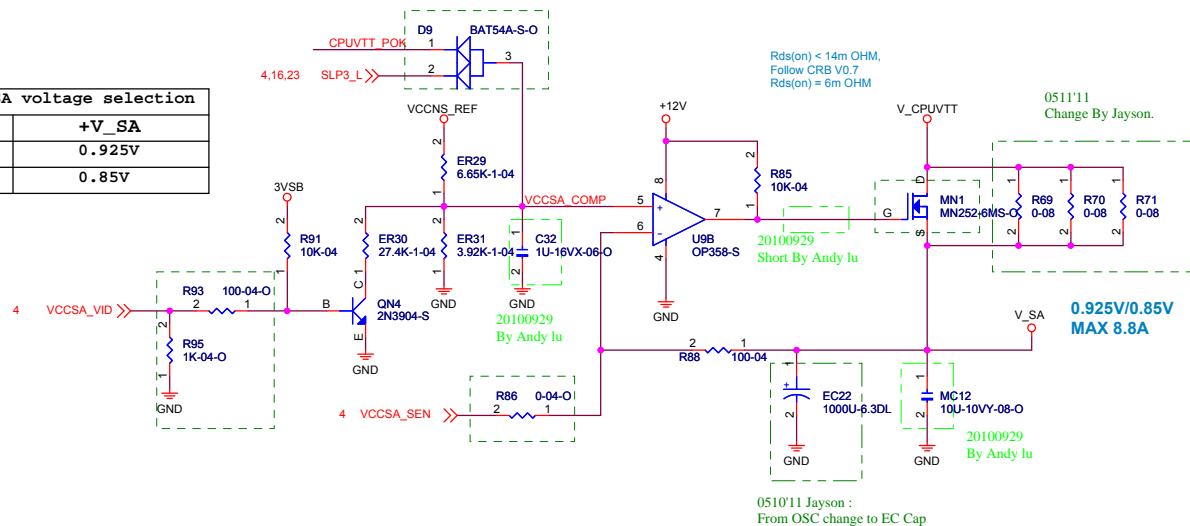
## External Connection



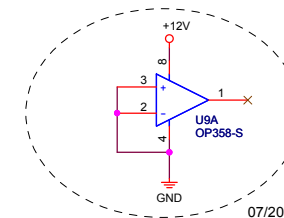
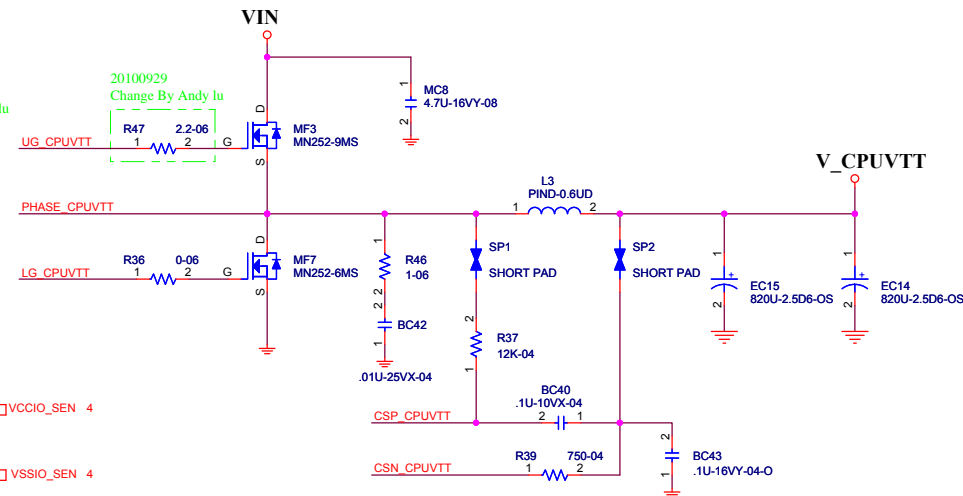
4 VTT\_SEL VID0



VID	+V_SA
0	0.925V
1	0.85V

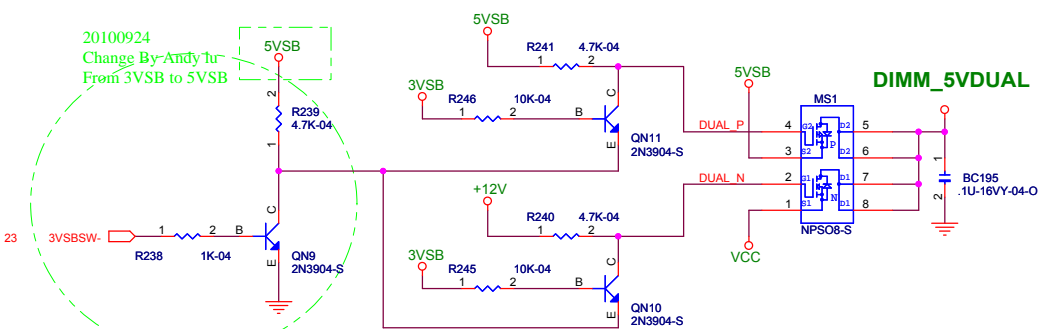


VID1	VID0	V_CPUVTT
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V

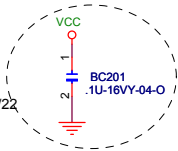


0525'11 Jayson :  
D13,R110,R114,R97,MN1先拿掉  
R276,R277,R278 上件 +

20100924  
Change By Andy lu  
From 3VSB to 5VSB

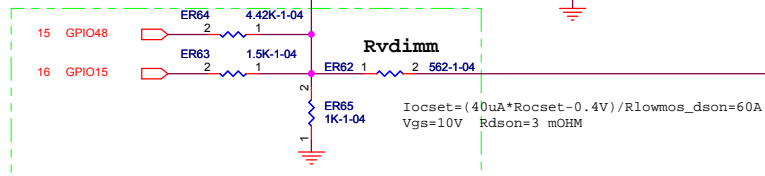


20100924  
Add By Andy lu  
For Fintek SIO



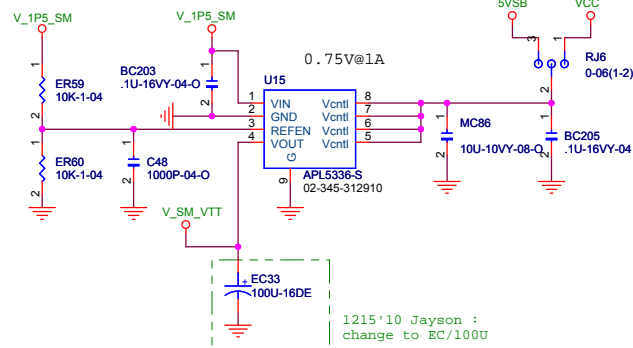
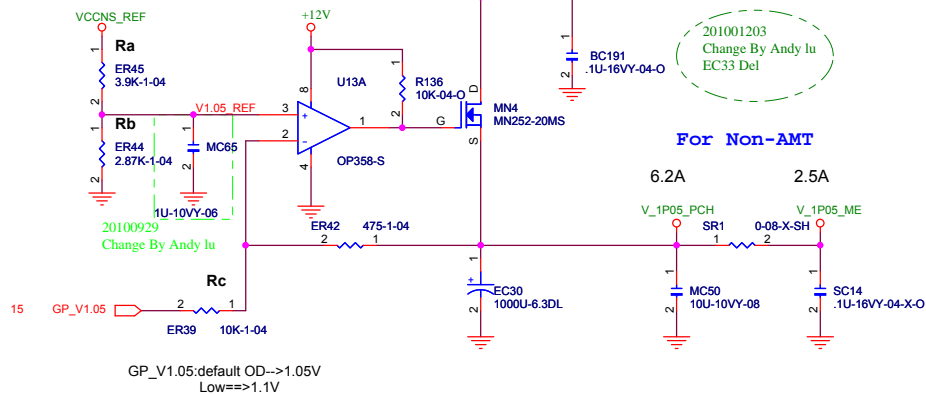
reserve for LG\_DIMM refer to VCC Jack 06/22

1207'10 Jayson :  
Add By Jayson  
for Down Voltage of DIMM



201001203  
Change By Andy lu  
EC33 Del

For Non-AMT

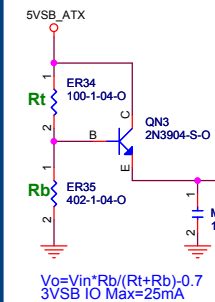


1215'10 Jayson :  
change to EC/100U

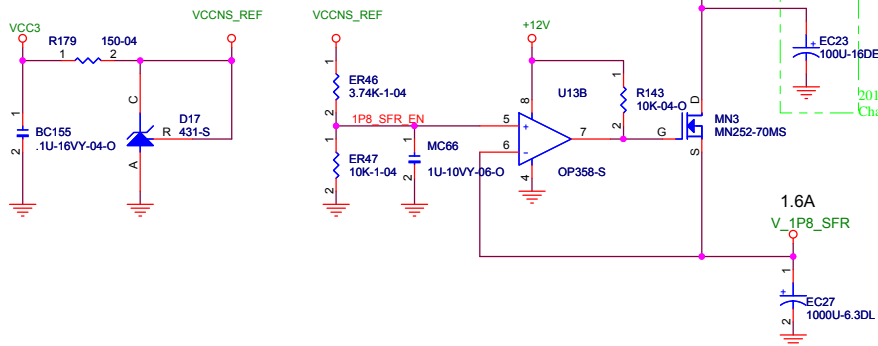
Refer to page28

Sd

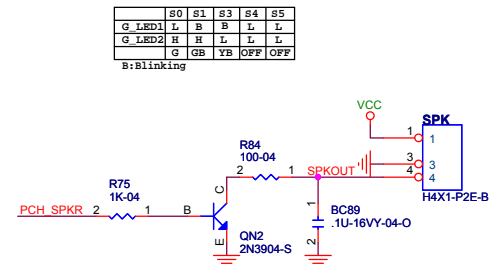
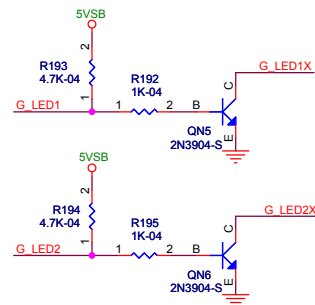
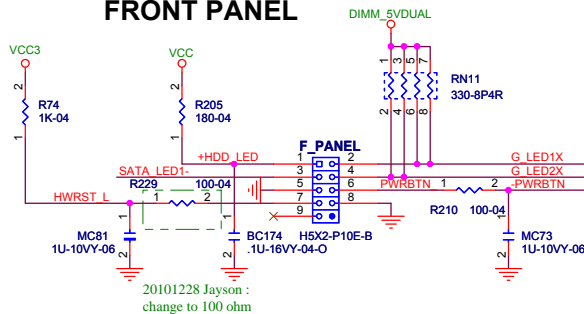
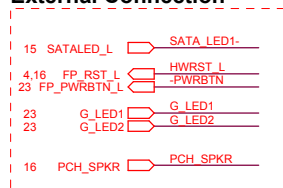
3VSB\_IO



1210'10 Jayson :  
3VSB\_IO 先線路預留不上  
,SIO有內轉power.



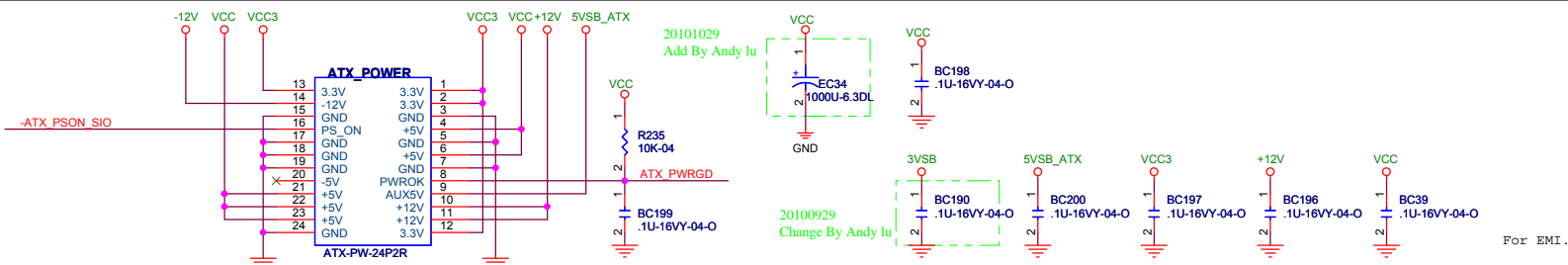
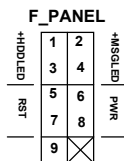
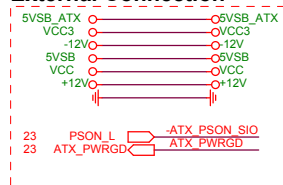
## FRONT PANEL



	S0	S1	S3	S4	S5
G LED1	L	B	B	L	
G LED2	H	H	L	L	
	G	GB	YB	OFF	C

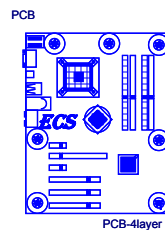
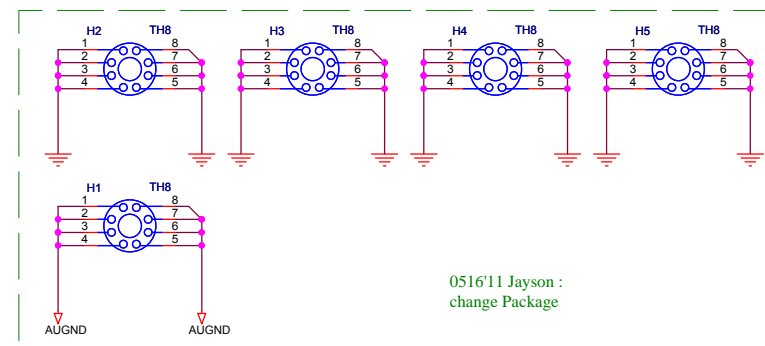
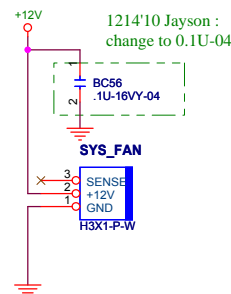
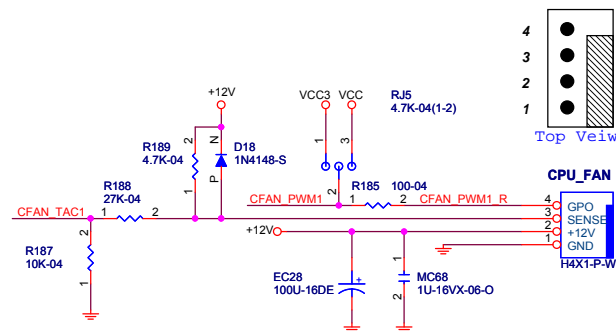
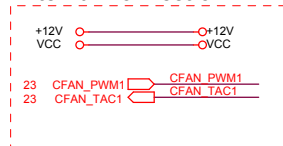
## POWER CONNECTOR

## External Connection

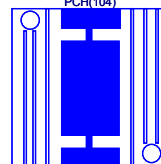


**FAN**

## External Connection



PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

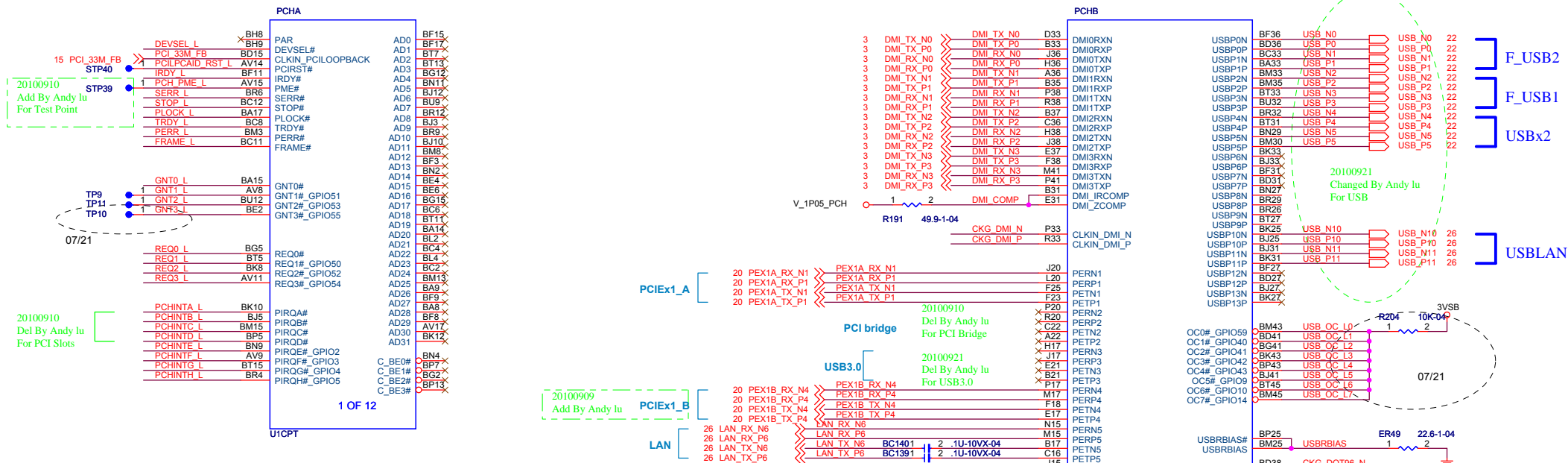


20-120-012242

5series PN:20-120-010851



For H61:USB Port 6/7/12/13 is disabled....From 440377 file



For H61:PCIE 7/8 is disable....From intel Jasmine

GPIO19:  
Boot Device Select Strap.

GNT0\_L:  
No More Information in EDS V0.7

GNT1\_L:  
Boot Device Select Strap.

GNT2\_L:  
ESI Strap ( Server Only),  
DON'T Pull Low in Desktop.

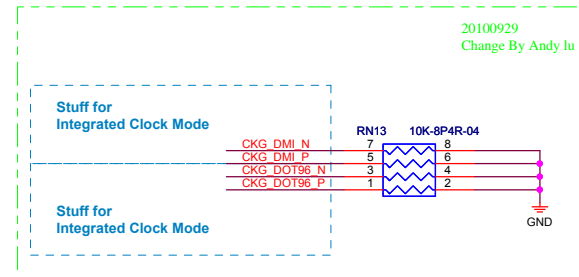
GNT3\_L:  
Top-Block Swap Override Mode,  
When Sampled Low.

**GNT[0..3]#**  
**GPIO19**  
have been internal pull high to +VCC3

**Boot Device Select:**

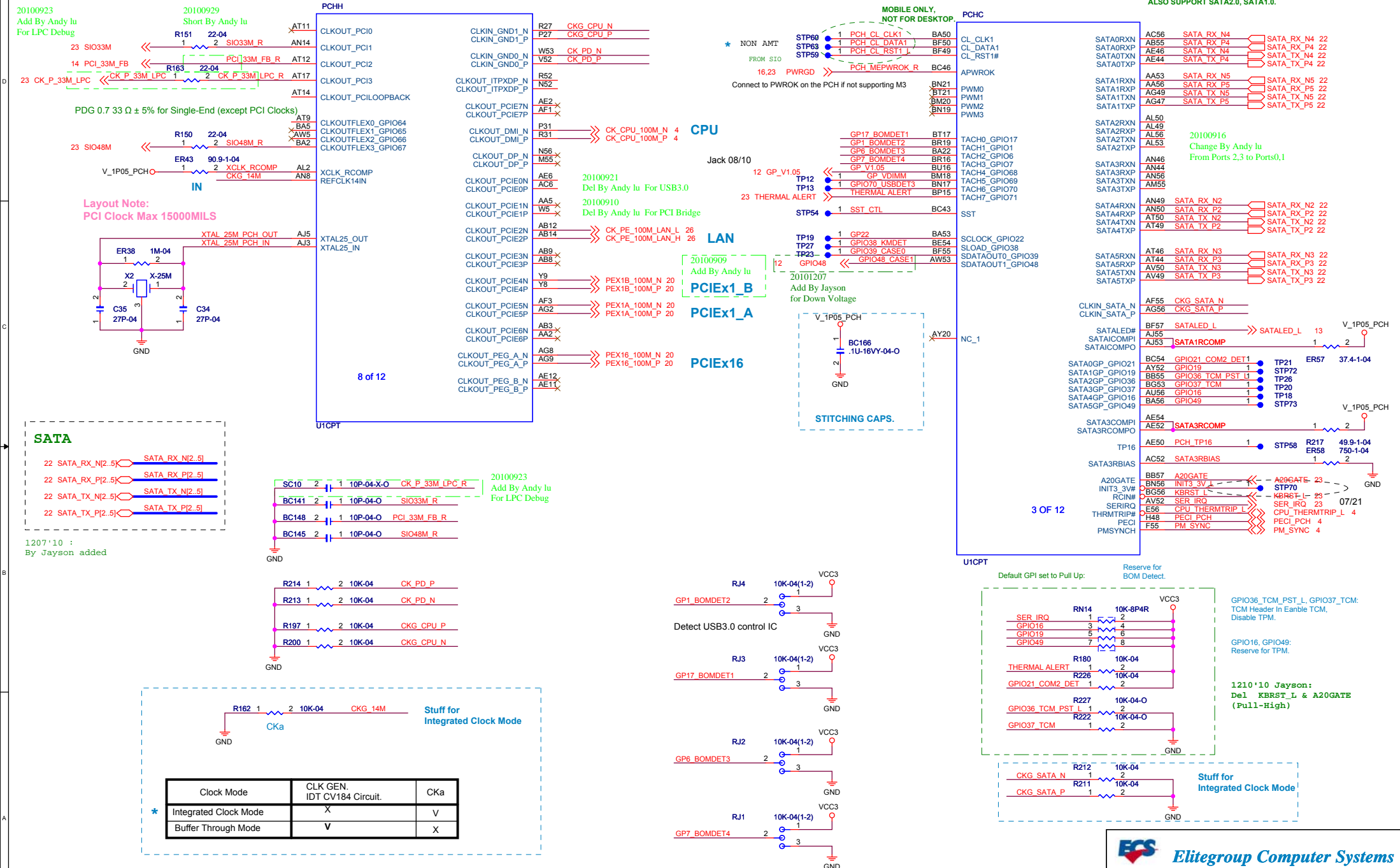
BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

\*

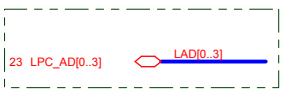


For H61:SATA port2/3 is disable....From 440377 file

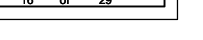
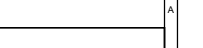
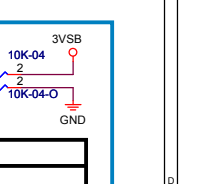
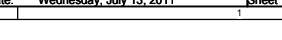
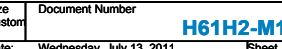
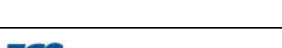
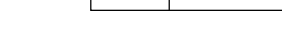
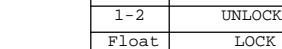
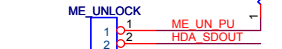
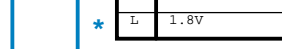
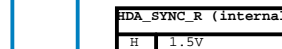
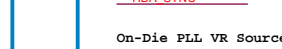
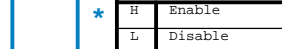
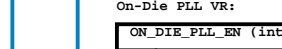
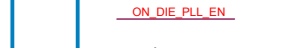
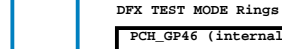
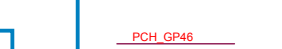
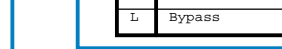
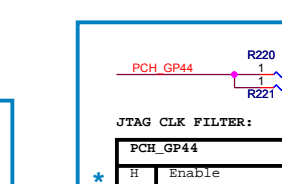
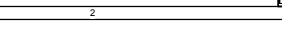
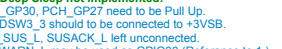
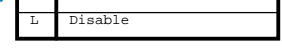
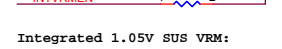
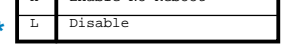
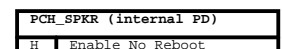
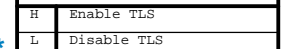
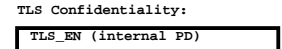
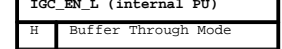
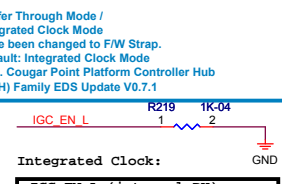
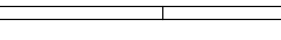
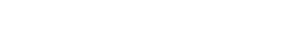
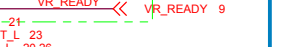
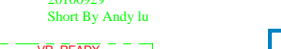
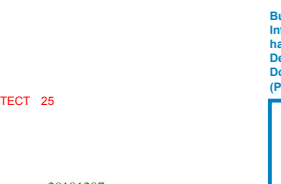
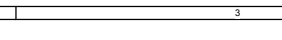
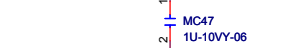
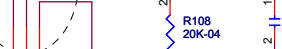
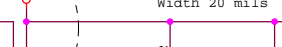
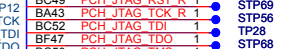
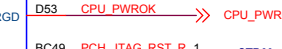
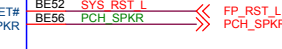
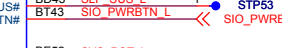
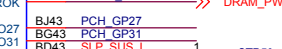
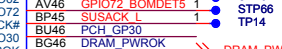
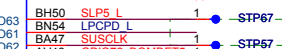
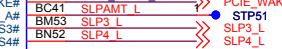
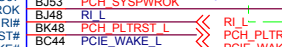
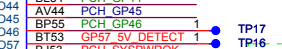
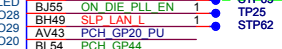
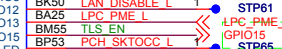
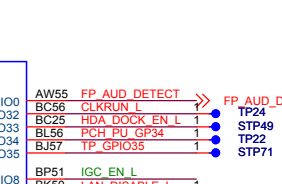
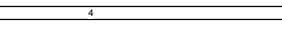
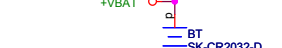
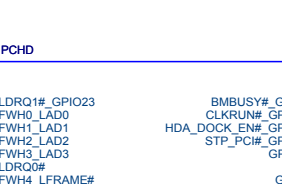
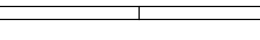
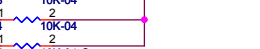
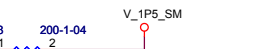
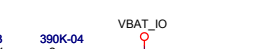
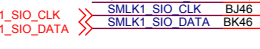
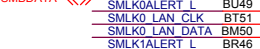
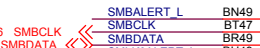
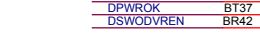
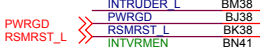
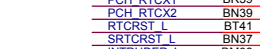
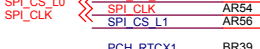
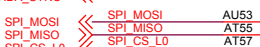
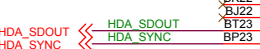
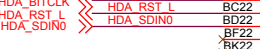
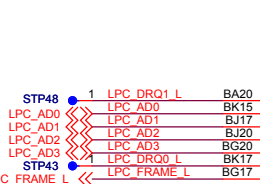
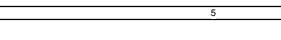
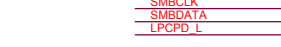
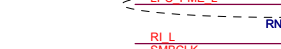
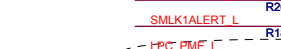
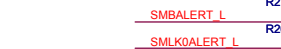
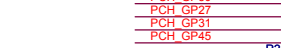
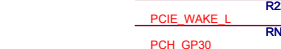
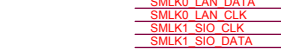
**ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,  
ALSO SUPPORT SATA2.0, SATA1.0.**



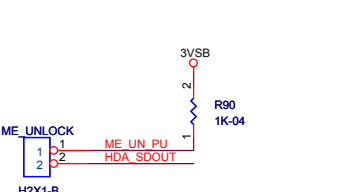
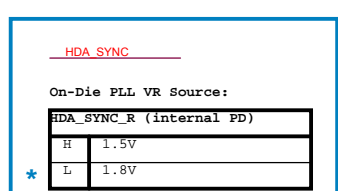
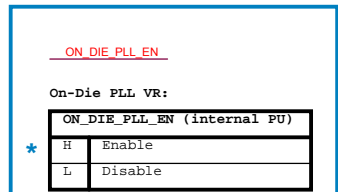
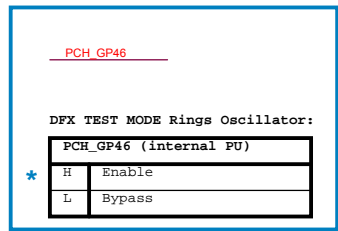
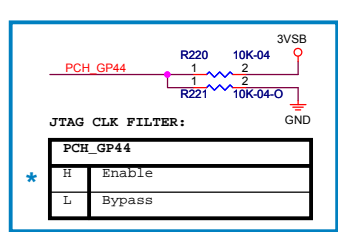
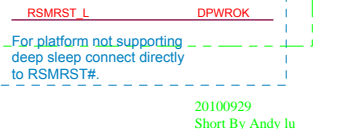
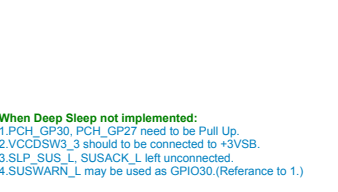
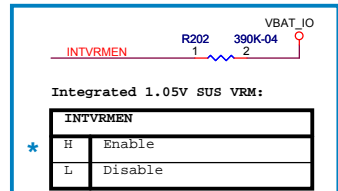
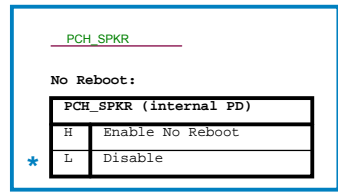
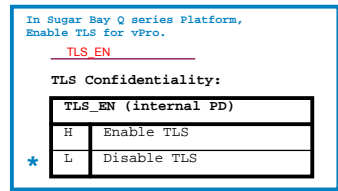
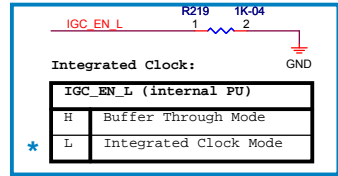




1207'10 :  
By Jayson added



Buffer Through Mode /  
Integrated Clock Mode  
have been changed to F/W Strap.  
Default: Integrated Clock Mode  
Doc. Cougar Point Platform Controller Hub  
(PCH) Family EDS Update V0.7.1

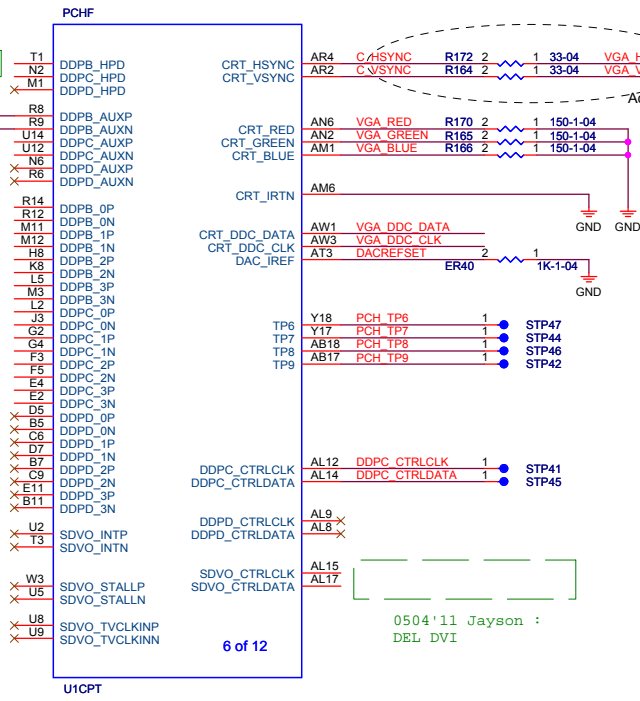


When Deep Sleep not implemented:  
1.PCH\_GP30, PCH\_GP27 need to be Pull Up.  
2.VCC0SV3\_3 should to be connected to +3VSB.  
3.SLP\_SUS\_L, SUSACK\_L left unconnected.  
4.SUSWARN\_L may be used as GPIO30.(Reference to 1.)

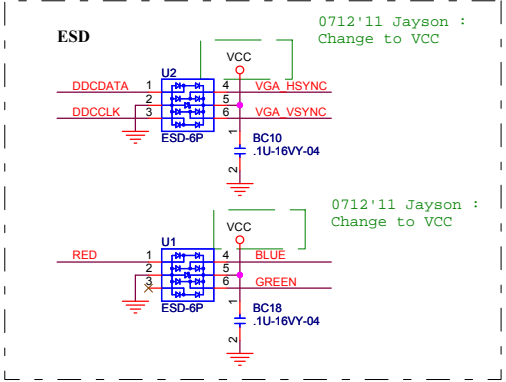
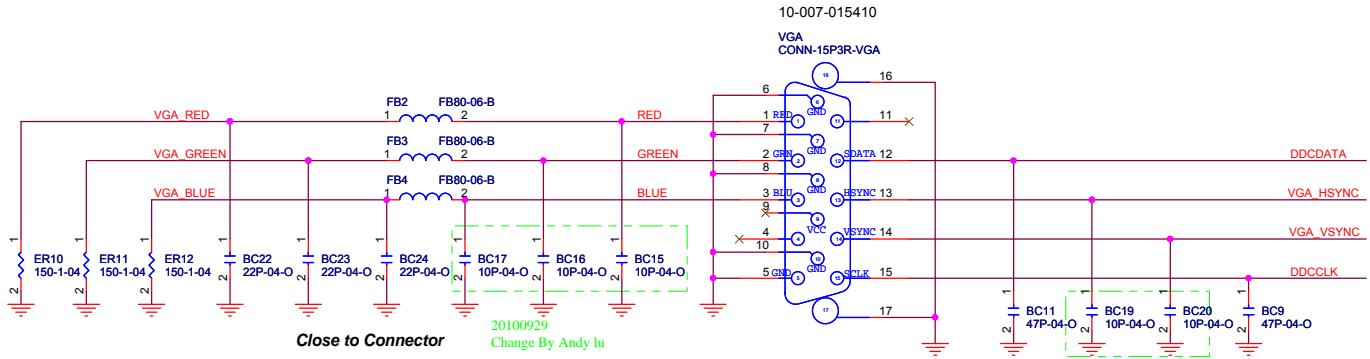
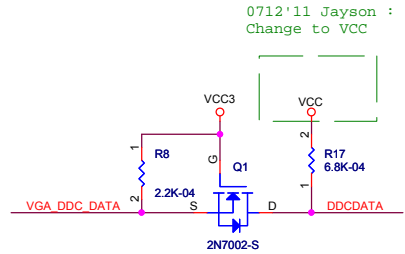
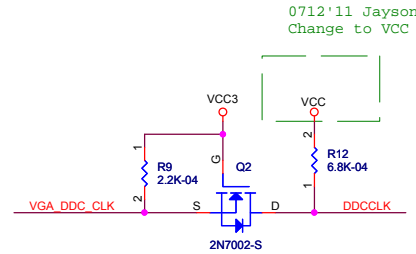
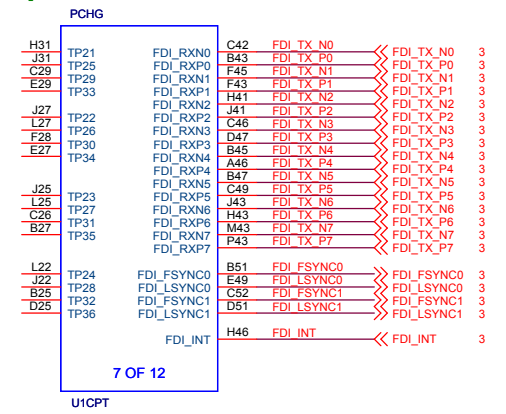
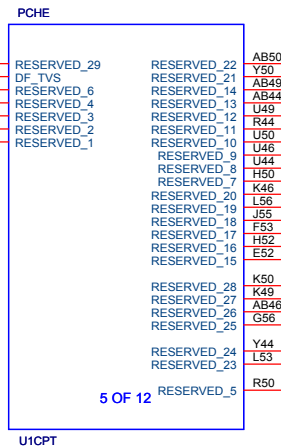
For platform not supporting  
deep sleep connect directly  
to RSMRST#.

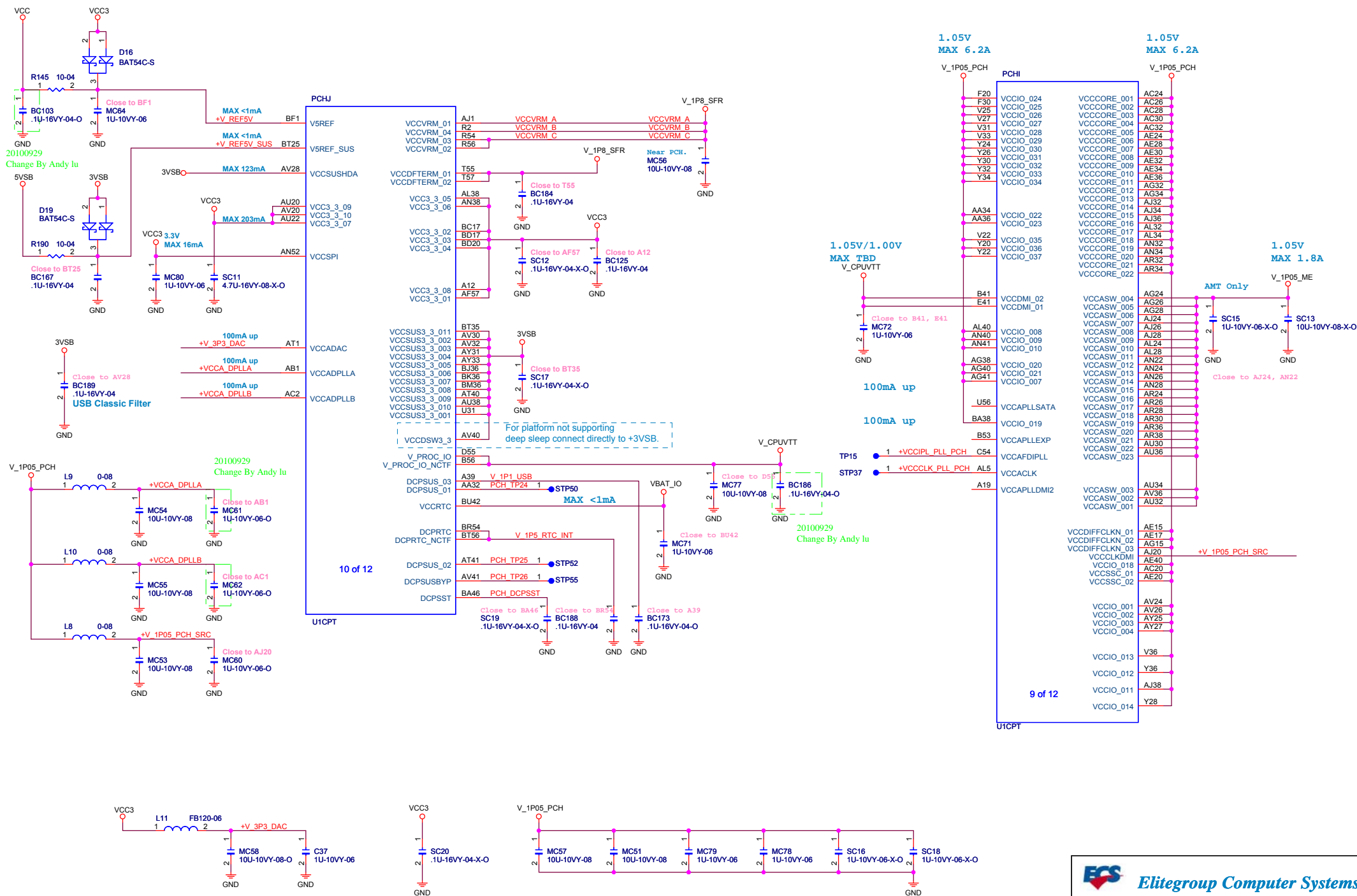
0504'11 Jayson :  
DEL DVI

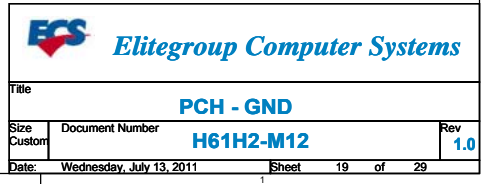
0504'11 Jayson :  
DEL DVI

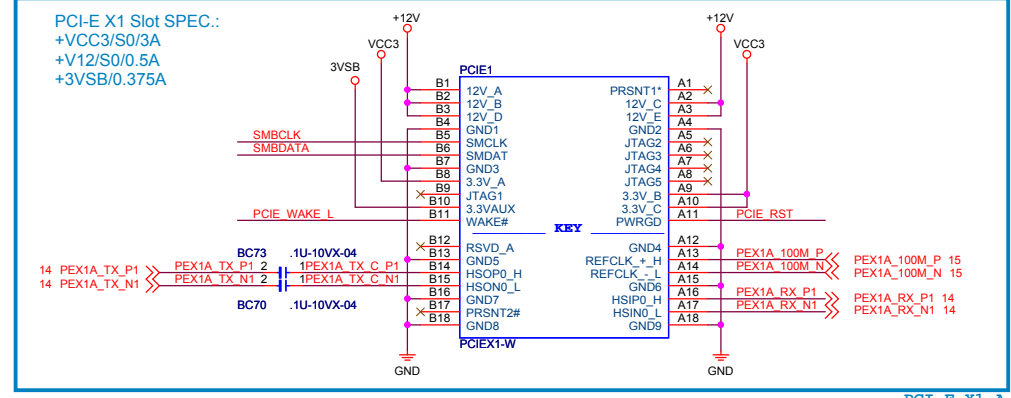
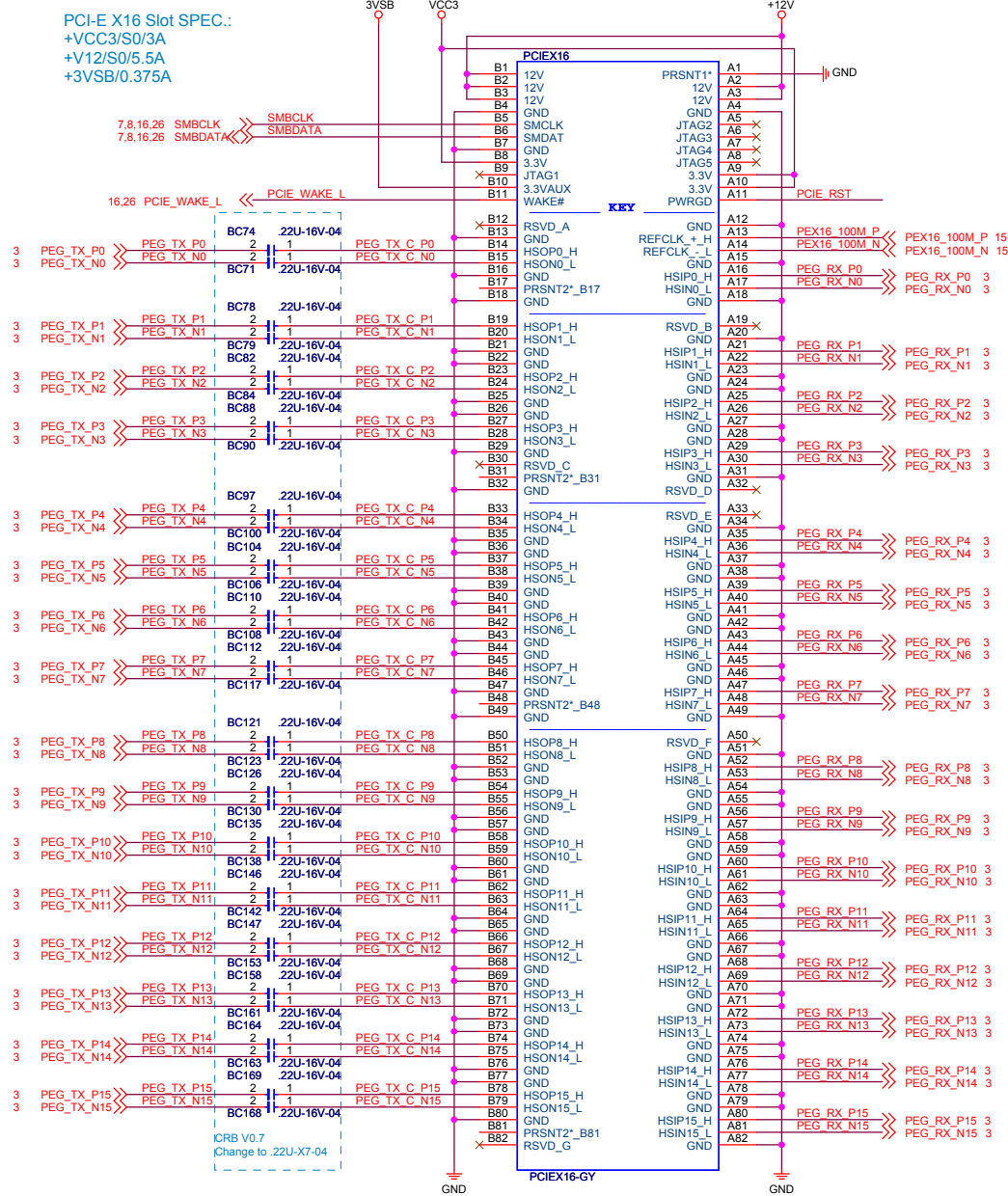


091222 Update!  
Terminating unused DC NAND interface:  
If not implemented, the dual channel NAND interface signals, including NV\_RCOMP, can be left as No Connect.  
Note:  
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.  
100120 Update!  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Rev1p0.zip:  
Renamed NV\_WE#\_CK[0:1], NV\_RE#\_WRB[0:1], NV\_RCOMP, NV\_RB#, NV\_DQ9 / NV\_IO[0:15], NV\_DQS[0:1], NV\_CE#[0:3], and NV\_ALE to Reserved(RSVD).  
Renamed NV\_CLE to DF\_TV5.

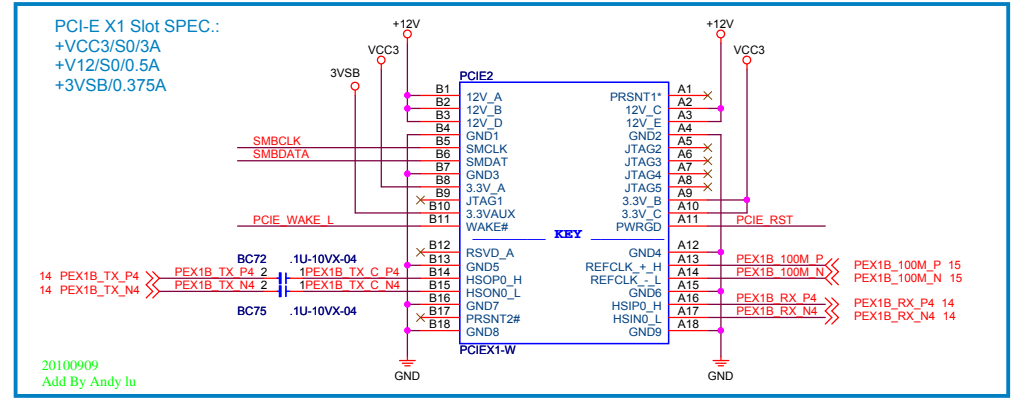








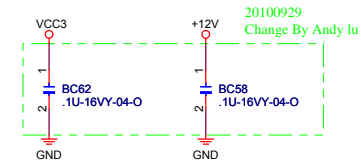
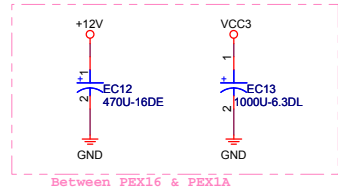
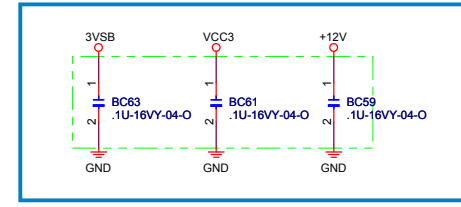
PCI-E X1 A



PCI-E X1 B

20100909  
Add By Andy lu

20100929  
Change By Andy lu



0504'11 Jayson :  
DEL DVI

0504'11 Jayson :  
DEL DVI

0504'11 Jayson :  
DEL DVI Connector

DVI

0504'11 Jayson :  
DEL DVI

0504'11 Jayson :  
DEL Fuse & Diode

0504'11 Jayson :  
DEL DVI

1202'10 Jayson :  
Del HDMI

USBVCC1

USBVCC1

USBVCC1

20100929  
Change By Andy lu

PS2

RN1  
4.7K-8P4R

BC31  
1U-16VY-04-O

PSKBM

PS2-KB-MS

FB8  
0-SH-06-O

FB7  
0-SH-06-O

FB10  
0-SH-06-O

FB9  
0-SH-06-O

CN1  
180P-8P4C

KBDATA  
NC1  
GND  
VCC  
KBCLK  
NC2  
MSDATA  
HOLE2  
HOLE3  
HOLE4  
HOLE5  
GND1  
VCC1  
MSCLK  
NC4

HOLE1  
HOLE2  
HOLE3  
HOLE4  
HOLE5

13  
14  
15  
16  
17

23  
KDATA  
KCLK  
MDATA  
MCLK

12V  
VCC  
-12V  
GND

1N4148-S

1N4148-S

ST75185CT-S

RY1  
RY2  
RY3  
RY4  
RY5

DA1  
DA2  
DA3  
DA4  
DA5

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
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NR3A  
NR4A  
NR5A

NR1A  
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NR5A

NR1A  
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NR5A

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NR5A

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

COM  
NR1A  
NR2A  
NR3A  
NR4A  
NR5A

H5X2-P10E-B

CN2  
180P-8P4C-O

CN3  
180P-8P4C-O

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
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NR5A

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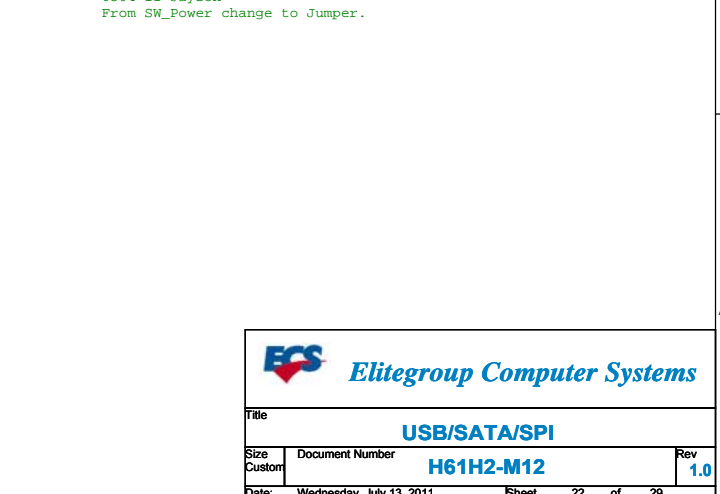
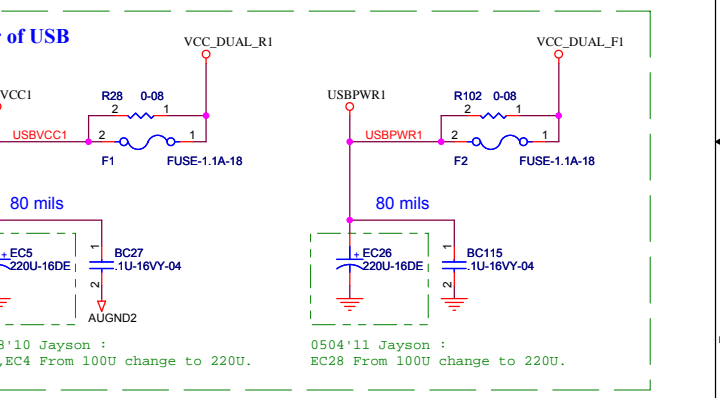
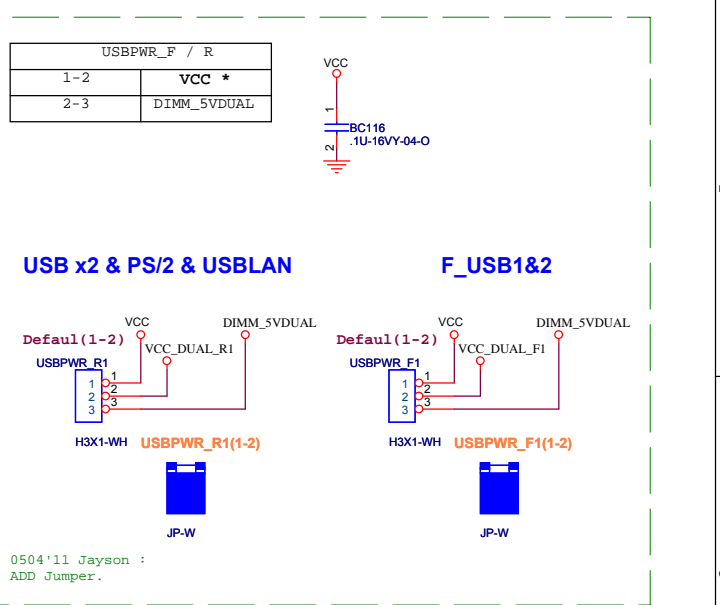
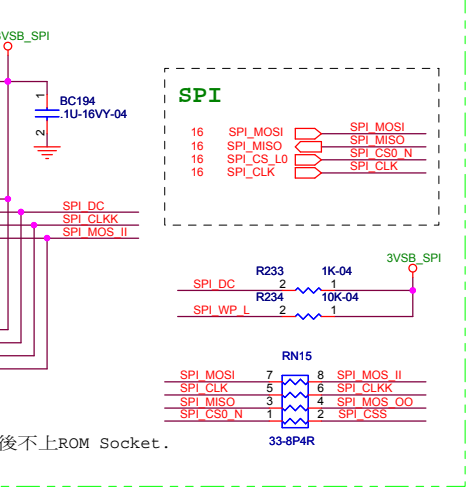
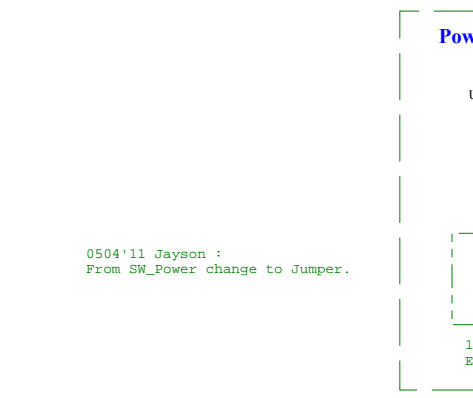
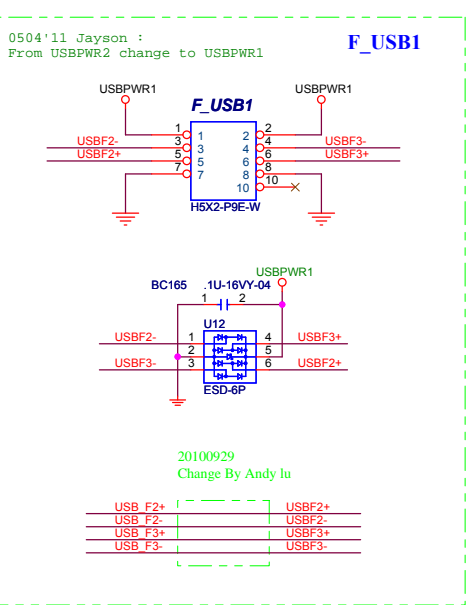
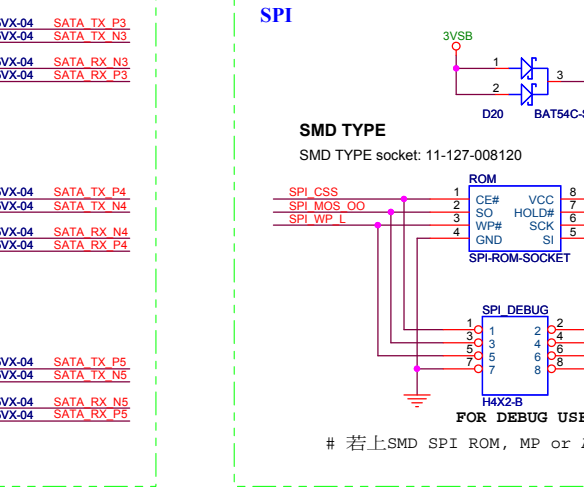
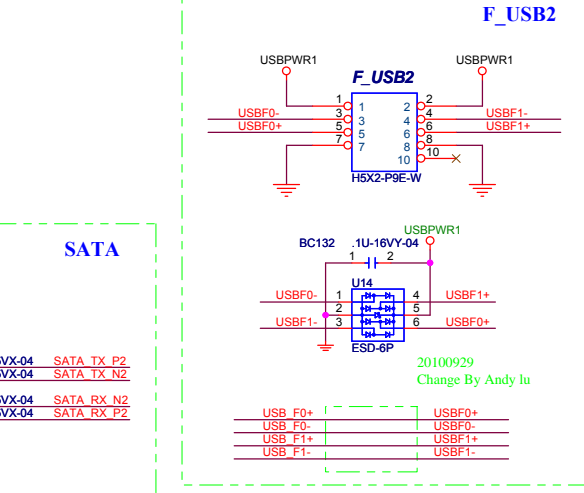
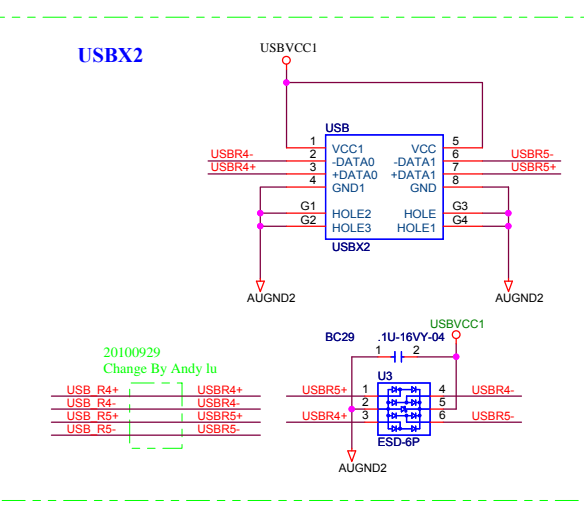
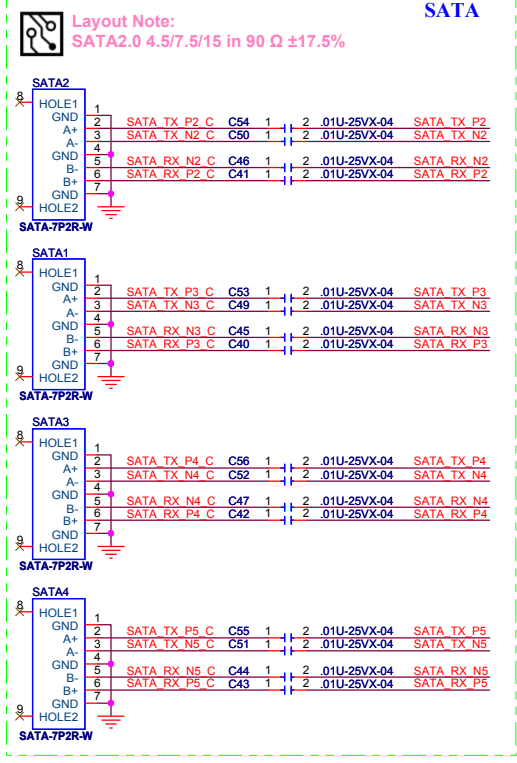
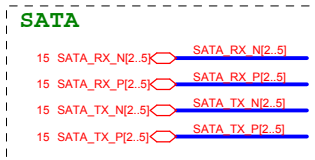
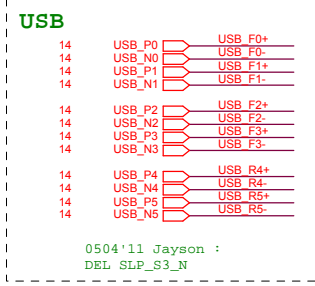
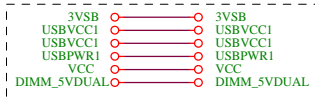
NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

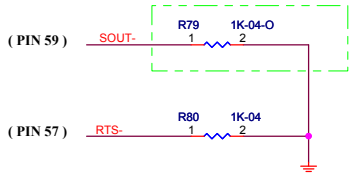
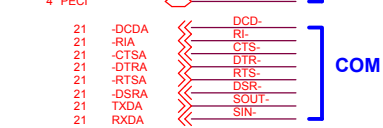
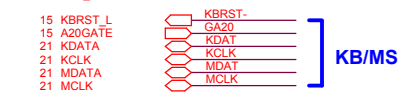
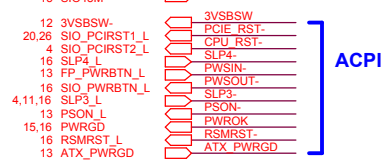
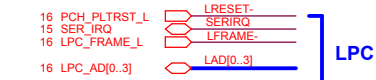
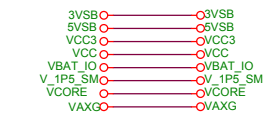
NR1A  
NR2A  
NR3A  
NR4A  
NR5A

NR1A  
NR2A  
NR3A  
NR4A  
NR5A

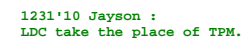




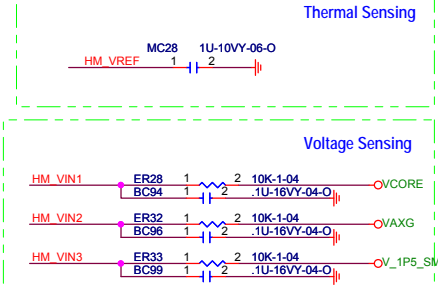
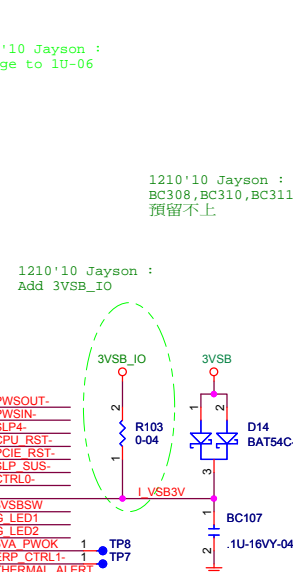
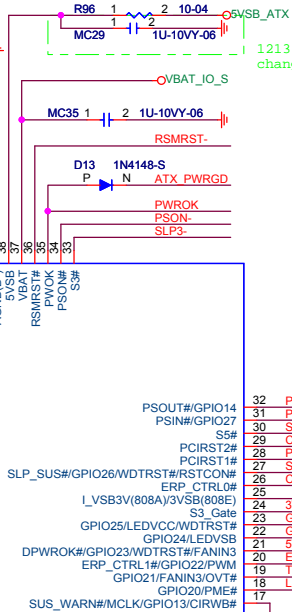
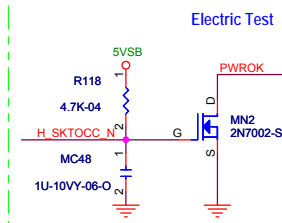
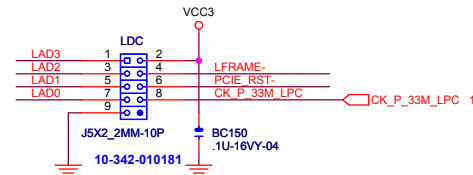
## External Connection



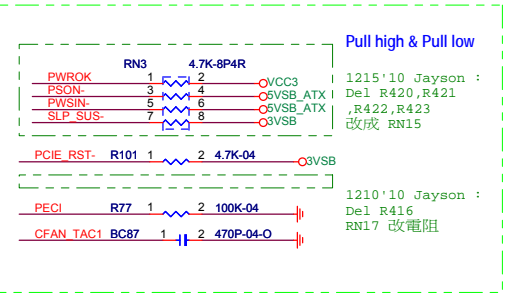
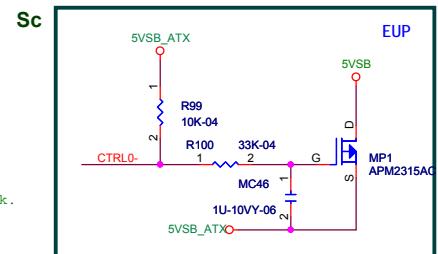
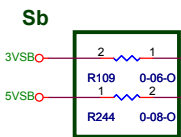
PIN NO.	Symbol	Value	Description
PIN 59	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.
PIN 57	STRAP_PWOK	1	PWOK(pin 35) for AMD(Default)
		0	PWOK(pin 35) for Intel



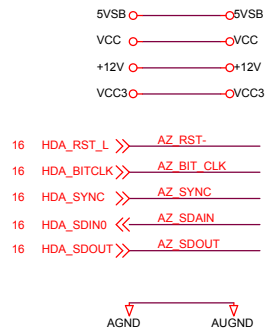
## LPC DEBUG HEADER



	W/O EUP	W EU
<b>Sb</b>	V	X
<b>Sc</b>	X	V
<b>Sd</b>	X	V



## External Connection

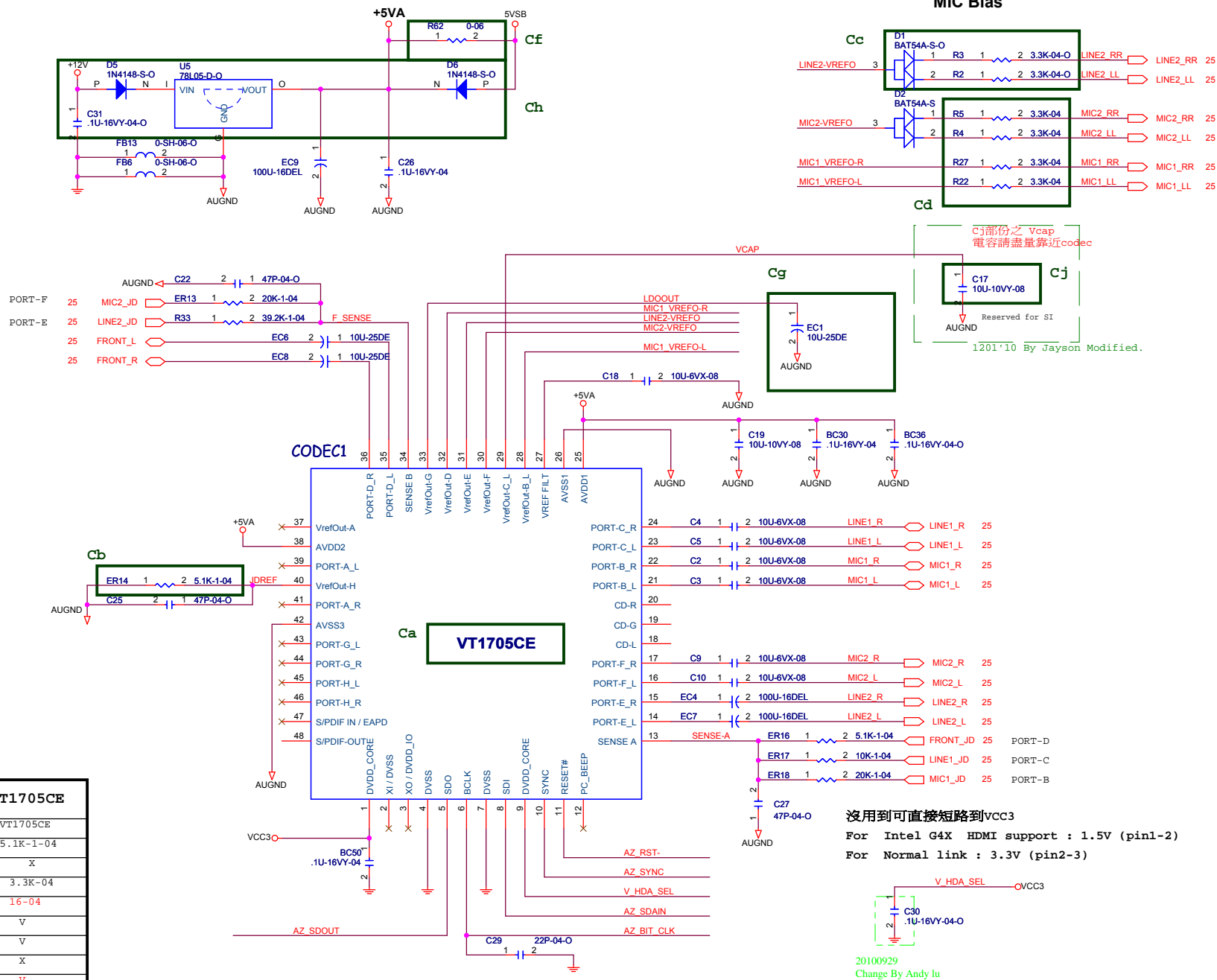


\* VCC1.5 can remove for non-Intel G4X platform

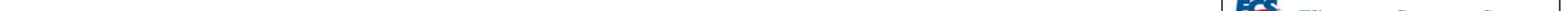
## BOM Difference

Location	ALC662	VT1705CD	VT1705CE
Ca	ALC662-VC-GRS	VT1705CD	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	16-04
Cf	X	X	V
Cg	X	V	V
Ch	V	V	X
Cj	X	X	V
Ck	75-04	33-04	33-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.



16 FP\_AUD\_DETECT << HDPANEL\_DETECT

[illegible]

1202'10 Jayson: C7 C8 AUDIO-3P-HDA R19 R18 C14 C13 C11 C12

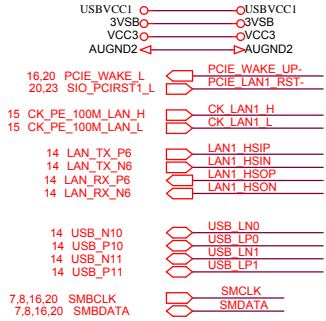


AUDIO VT1705/ALC662 (PANEL)

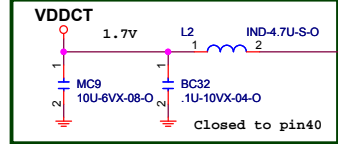
[illegible]

5	4	3	2	1
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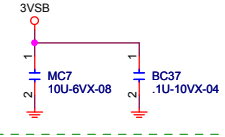
## External Connection



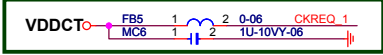
Ch



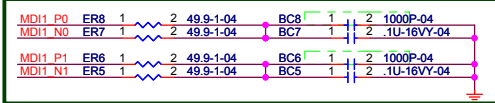
Closed To Pin1



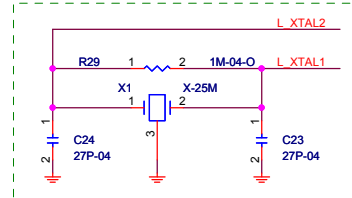
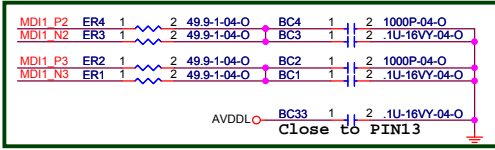
Ch



Ci



Cg

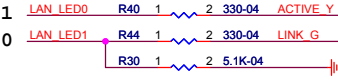


## BOM Difference

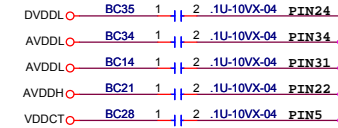
	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Ch	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

## HW Strapping

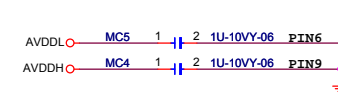
LED0 : 0 -> OC disable  
1 -> OC enable  
LED1 : 0 -> VDDCT\_REG enable  
1 -> VDDCT\_REG disable



## Closed To PWR Loading Pin



## Closed To PWR Source Pin



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Change By Andy lu

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ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching UP6230 4 hases
--------------------------------

Vcore:0.65~1.3V 11.2Amax

Vauxg:0.65~1.3V 35Amax

Switching OP6123 1 phase
--------------------------------

V\_CPU\_VTT:1.05V 1.7Amax

Linear OP358
-----------------

VCC\_SA:0.925V(0.85V) 8.8Amax

Switching APW 7120
-----------------------

V\_DIMM:1.5V 28.5Amax

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S3
V_SM_VTT	1.0A_S0

DDR\_VTT:0.75V

LDO APL5336
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Linear OP358
-----------------

PCH\_CORE:1.05V 6.2Amax

Non AMT:  
VccASW(ME) short to V1P05\_PCH

V\_ME:1.05V 1.8Amax

Linear OP358
-----------------

V\_SFR:1.8V 1.6Amax

Not support DSW mode:  
VccDSW short to 3VSB

Intel Sandy Bridge CPU		
VCCP	V1D 0.25~1.52V	85A(95W)
VAXG	V1D 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLL	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUS3_3	3.3V	0.097A
VccSUS3_3	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

Battery  
3V

NEC_D720200		
VDD3P3	3.3V	TBD
VDD1P05	1V	TBD
CTRL1P0 internal LVR Output		

SUPER I/O F71808A		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO VT1705CE		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

Total 2 Slots

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

Total 1 Slot

USB X4 Header	
VDD	5VDual
2.0A	2.0A

USB X4 IO	
VDD	5VDual
2.0A	2.0A

USB3.0	
5VDual	2A



**NOTE:**  
Sugar Bay Platform has two clock mode:  
1.Integrated Clock Mode (Generate by PCH)  
2.Buffer Through Mode (Generate by Clock Gen.)  
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.  
Please refer to  
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD  
Page.13 PCH - SATA, SATA CONN for CLK IN PD  
Page.14 PCH - MISC, F/W Strap  
Page.15 PCH - CLK IO, CKG - CV184 for Option

1129'10 By Jayson Del CK505

1129'10 By Jayson modified

